

REMARKS

Claims 1-6 and 8-20 are pending in the above-identified application. Claims 1-6 and 8-20 were rejected. Each of the rejections is respectfully traversed.

35 U.S.C. § 102 Anticipation Rejection of Claims

Claims 1-6, and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Matthies et al.* (U.S. Patent No. 6,476,783). Applicants respectfully traverses this rejection.

First, *Matthies* fails to teach a "glass substrate provided with through-holes" as recited in claim 1. The Examiner points to element 110 in Figures 19 and 20 as purportedly disclosing this limitations. The Examiner is mistaken. *Matties* simply states that element 110 is an "insulating substrate" (Col. 17, lines 61-62). *Matties* makes absolutely no suggestion that this layer is glass. The only layer taught by *Mathies* that is formed of glass is layer 120. However, this layer is a cover, and as can be seen from Figs. 19 and 20, has no through-holes.

Second, *Matthies* also fails to teach "a sealing member provided to fill said through-holes, said sealing member being operable to inhibit moisture permeation through said through-holes." The Examiner asserts that this limitation is disclosed at column 17, line 65 to column 18, line 15. Again, the Examiner is mistaken. *Matthies* simply teaches that electronics section 102, as a whole, functions as a barrier layer. *Matthies* also states that an epoxy resin is used to join the display and circuit board layers. However, *Matthies* does not disclose or even suggest that the through-holes in layer 110 (which as discussed above, is not a glass substrate) are filled with a sealing member.

Accordingly, Applicant submits that independent claim 1, as well as dependent claims 2-6, and 8 are allowable over the cited references.

35 U.S.C. § 103 Obviousness Rejection of Claims

Claims 9-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Matthies et al.* in view of *Nakazawa et al.* (U.S. Patent No. 6,411,349). Applicants respectfully traverse this rejection.

With regards to claims 9-20, the Examiner asserts that *Matthies* discloses each claim element except for "a second sealing member provided in such a manner as to surround a display device while being in contact with a printed wiring board and a protective glass board." For this element, the Examiner instead relies on *Nakazawa*.

First, as discussed above for claim 1, *Matties* fails to teach a "glass substrate provided with through-holes." As independent claims 9 and 15 each also recite "a glass substrate provided with through-holes", these claims are allowable for at least the same reasons as discussed above for claim 1.

Second, Applicant also submits that *Nakazawa* does not teach "a second sealing member provided in such a manner as to surround a display device while being in contact with a printed wiring board and a protective glass board." *Nakazawa* discloses a peripheral seal section 252. This section is positioned on the same layer as liquid crystal layer 225, and is sandwiched between electrode 224 and the pixel electrodes 12. Thus, the seal section in *Nakazawa* is not in contact with both a printed wiring board and a protective glass board, as recited in claims 9 and 15. Accordingly, independent claims 9 and 15, as well as dependent claims 10-14 and 16-20 are allowable over the cited references.

In view of the foregoing, Applicants submit that the application is in condition for allowance. Notice to that effect is requested.

Respectfully submitted,

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